EASTERN UNIVERSITY, SRI LANKA
DEPARTMENT OF MATHEMATICS
CIAL DEGREE EXAMINATION IN COMPUTER SCIENCE, 2013/2014 (October, 2016)
CSS03: Advanced Computer Architecture
Answer all questions
This paper has 6 questions in a total of 3 pages

allowed: **Three Hours**

he Von Neumann architecture defines the structure of a computer as well as the way it processes formation.

a) Draw a block diagram of a CPU and name the components. Give a short description of each of the components. [20%]

b) Write down the sequence of operations performed by the CPU during its execution of instructions (CPU instruction cycle). [20%]

c) Memory read and memory write are the two basic memory operations.

i. State the steps that a CPU performs for a *memory read* operation. [30%]

ii. State the steps that a CPU performs for a *memory write* operation. [30%]

gisters are important functional components of a processor.

a) State what is a register an d their functionality in a processor. [20%]

b) List for special purpose registers found in a processor and describe their purpose. [23%]

c) Considering the following memory arrangement, write all the intermediate steps taken to execute the instructions starting from memory location 1000. [50%]

Data segment

Address	Content	Assigned Variable name
...	....	....
100	53	A
101	63	B
102	0	SUM
...	....	....

Code segment

Address	Content	Meaning
...	....	....
1000	Load AX, SUM	Copy the value of SUM into AX
1001	Add AX, 100	AX = AX + 100
1002	Store AX, A	Copy the value of AX into A

struction set architecture (ISA), is the part of the computer architecture related to programming.

b) Describe briefly each of the following *addressing modes*, with the aid of suitable examples[25%]

i. Immediate ii. Direct (Absolute) iii. Register indirect
iv. Memory indirect v. Indexed

[Question 3 continues on the next page]

(b) Describe the purpose of the following instruction types with the aid of two instructions each type.

i. Data movement instructions ii. Arithmetic and Logical instructions

(c) Describe how sequencing happens in instruction execution of a processor using a suit example.

(d) Consider a CPU that has a number of registers including R0, R1 and R2. Value stor register R0 is 500 and in R1 is 1500. Describe the following operations and the outcom each operation (assume that all numbers are decimal).

1. LOAD #5000, R2
2. ADD (R0)-, R2
3. SUBTRACT +(R1), R2
4. MOVE 100(R0), R2
5. STORE R0, 100(R2)

4. Sequencing is an important aspect of a computer programme.

(a) List two Sequencing instructions and state their purpose.

(b) Describe how sequencing happens in instruction execution of a processor using a s example.

(c) Convert the following high level language programme into a low level language.

```
sum = 0;
for i= 1 to 10
sum = sum + A[i];
next i
```

5. The primary function of a CPU is to execute a set of instructions stored in the computer m

(a) Draw the *system bus model* of a computer system and describe the functions of ea ponent briefly.

(b) Draw and name the components of a *two-bus organization* of a CPU.

(c) The instruction `Add X,R0` adds the contents of memory location `X` to register R_0 an the result in R_0. Write the sequence of events in executing this instruction.

(d) State how the instruction `Add X,R0` can be accomplished in the two-bus organiza have described in part (b).

emory of a computer is organised in hierarchy to make a computer more cost effective and ficient.

a) Describe briefly the memory hierarchy found in a typical computer and explain how it improves the performance of a computer. [15%]

b) Describe *temporal locality* and *spatial locality*. In addition describe how these concepts are used to improve the performance of a processor. [20%]

c) Describe the memory address structure for each of the following mapping techniques: [30%]

i. Direct mapping ii. Associative mapping

iii. Set associative mapping

d) Consider a main memory consisting of 4K blocks, a cache memory consisting of 256 blocks. Determine the number of bits in each field of the address in each of the following organizations:

i. Direct mapping with block size of eight words. [15%]

ii. Associative mapping with a block size of sixteen words. [20%]

End