EASTERN UNIVERSITY, SRI LANKA
FIRST EXAMINATION IN SCIENCE 2003/2004 (Repeat)
SECOND SEMESTER (June/July, 2005)
CS106 - Computer Organization and Architecture
Answer All Questions

Time Allowed: Two hours

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1. State and prove De Morgon's Theorem.

   (a) Prove that $(A+B).(\overline{AB}) = A.\overline{B} + \overline{A}.B$

   (b) Simplify the following expressions:

   i. $\overline{\overline{A+B.\overline{C}+D.\overline{(E+\overline{F})}}}$

   ii. $\overline{A}.\overline{B}.\overline{C}.\overline{D} + \overline{A}.B.\overline{C}.\overline{D} + A.B.\overline{C}.D + A.\overline{B}.\overline{C}.D + A.B.C.D + A.\overline{B}.C.D + \overline{A}.\overline{B}.C.\overline{D} + \overline{A}.B.C.\overline{D} + A.B.C.\overline{D} + A.\overline{B}.C.\overline{D}$

   (c) Construct RS latch using NOR gates and describe its function.

   (d) A circuit has four inputs A, B, C, and D representing the sixteen natural binary integers 0000_2 to 1111_2. A is the most significant bit and D is the least significant bit. The output of the circuit, F, is true if the input is divisible by multiple of 4, 5, 6 or 7, with the exception of 15, in which case the output is false. Zero is not divisible by 4, 5, 7 or 7.

   i. Draw a truth table to represent the algorithm.

   ii. From the truth table obtain an expression for F and show that $F = \overline{A}.B + A.\overline{D}$

2. (a) Describe with the aid of examples, the properties of 2's complem numbers.

What is the range of 2's complement numbers in '**n**' bits and wh will happen if we violate this range? Provide examples.

(b) Explain the meaning of the following terms in the floating-point re resentation:

i. excess notation

ii. normalized mantissa

iii. hidden bit

(c) Describe the single precision IEEE floating-point representation.

Represent the following decimal numbers into single-precision (IE 32-bit) floating-point numbers:

i. -125.375

ii. 0.001

Convert the following single precision (IEEE 32-bit) floating-po numbers into decimal numbers:

i. 0 10000010 10010000000000000000000

ii. 1 01111110 11000000000000000000000

4.

3. (a) Describe the functions of the following registers in a computer:

- Program Counter (PC)
- Accumulator (ACC)
- Instruction Register (IR)
- Memory Address Register
- Memory Buffer Register

(b) Explain the steps involved in instruction execution.

(c) Partial list of 'Opcodes' of a hypothetical machine are given below:
0001 = load accumulator from memory
0010 = store accumulator to memory
0101 = add to accumulator from memory

Show the relevant portions of memory and CPU registers for the addition of two numbers located in the memory at the addresses 550_{16} and 551_{16} and stores the result in the later location.

(d) Describe the advantages and disadvantages of micro programming.

With the aid of a block diagram, describe a micro programmed control unit, explaining various elements involved.

4. (a) Illustrate, with the aid of a block diagram, the use of **Cache Memory** in alleviating the speed mismatch of memory and processors. Explain the terms **spatial locality** and **temporal locality** of reference of instructions in programs.

(b) Draw a schematic diagram for a **DMA** transfer from input to memory and describe the steps involved in the **DMA** transfer of one word.

(c) Describe the steps involved in interrupt servicing routine to cater to the I/O requirement.

(d) Describe the two ways to handle multiple interrupts.