EASTERN UNIVERSITY, SRI LANKA
FIRST EXAMINATION IN SCIENCE 2003/2004
SECOND SEMESTER (June/July, 2005)
CS106 - Computer Organization and Architecture
Answer All Questions

Time Allowed: Two hours

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1. State and prove De Morgan's Theorem.

(a) Prove that $(A+B).(\overline{AB}) = A.\overline{B} + \overline{A}.B$

(b) Simplify the following expressions:

i. $\overline{\overline{A+B.\overline{C}}+\overline{D.(E+\overline{F})}}$

ii. $\overline{A}.\overline{B}.\overline{C}.\overline{D} + \overline{A}.B.\overline{C}.\overline{D} + A.B.\overline{C}.D + A.\overline{B}.\overline{C}.D +$
$A.B.C.D + A.\overline{B}.C.D + \overline{A}.\overline{B}.C.\overline{D} + \overline{A}.B.C.\overline{D} +$
$A.B.C.\overline{D} + A.\overline{B}.C.\overline{D}$

(c) Construct RS latch using NOR gates and describe its function.

(d) A circuit has four inputs A, B, C, and D representing the sixteen natural binary integers 0000_2 to 1111_2. A is the most significant bit and D is the least significant bit. The output of the circuit, F, is true if the input is divisible by multiple of 4, 5, 6 or 7, with the exception of 15, in which case the output is false. Zero is not divisible by 4, 5, 7 or 7.

i. Draw a truth table to represent the algorithm.

ii. From the truth table obtain an expression for F and show that $F = \overline{A}.B + A.\overline{D}$

2. (a) Explain the meaning of the following terms in the floating-poi resentation:

    i. excess notation

    ii. normalized mantissa

    iii. hidden bit

(b) Describe the single precision IEEE floating-point representatio

Represent the following decimal numbers into single-precision (32-bit) floating-point numbers:

i. -125.375

ii. 0.001

Convert the following single precision (IEEE 32-bit) floating numbers into decimal numbers:

i. 0 10000010 10010000000000000000000

ii. 1 01111110 11000000000000000000000

(c) Draw a flow chart for the multiplication of two positive binary bers.

Perform the following multiplication, $3_{10} \times 4_{10}$.

(d) Draw a flow chart for the multiplication of two binary numbers, w one of the two given numbers is negative (Booth's method).

Perform the following multiplication, $2_{10} \times (-3)_{10}$.

3. (a) Describe the functions of the following registers in a computer:

- Program Counter (PC)
- Accumulator (ACC)
- Instruction Register (IR)
- Memory Address Register
- Memory Buffer Register

(b) Explain the steps involved in instruction execution.

(c) Partial list of 'Opcodes' of a hypothetical machine are given below:

0001 = load accumulator from memory
0010 = store accumulator to memory
0101 = add to accumulator from memory

Show the relevant portions of memory and CPU registers for the addition of two numbers located in the memory at the addresses 550_{16} and 551_{16} and stores the result in the later location.

(d) Suppose you are given a computer with the following 7 instructions:

POP A // Popping from the stack and store it in A
PUSH A // Pushing A into the stack
MUL // Multiply the two elements on the top of the stack and push the result onto the stack
DIV // Divide the top element by the next element and push the result onto the stack
IN A // Read from an input unit and store at the address A
OUT A // Out put the content of A to an output unit
HALT // Stop the execution

Write a program to this computer to do the following tasks:

i. read three numbers A, B and C.

ii. compute $Z = \frac{AX}{B}$, where$X = \frac{AC}{B}$

iii. output Z.

4. (a) Illustrate, with the aid of a block diagram, the use of **Cache M** in alleviating the speed mismatch of memory and processors. E the terms **spatial locality** and **temporal locality** of referenc structions in programs.

(b) Describe the I/O to processor communication in a computer sy

(c) Describe the steps involved in interrupt servicing routine to c the I/O requirement.

(d) Describe the two ways to handle multiple interrupts.