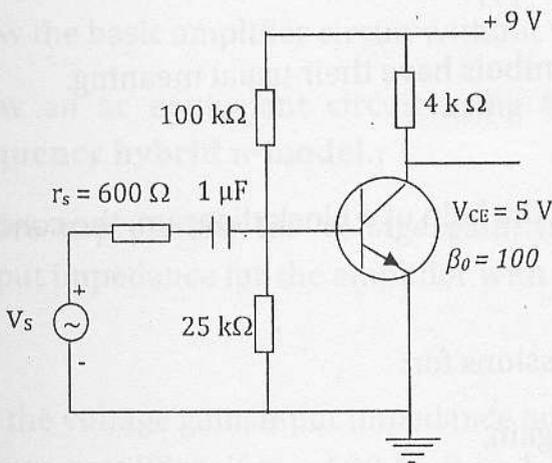


Time: 03 Hours.

Answer ALL Questions

1.



(a) Estimate the dc collector current of the above transistor amplifier and hence estimate the transistor parameters g_m and r_π .

(b) Draw the high frequency hybrid- π model of the above circuit with internal capacitors C_π , C_μ and resistors r_x , r_π .

You may assume that the capacitors C_1 and C_2 act as short circuits at high frequencies and neglect the effect of bias resistors R_1 and R_2 .

(c) Redraw the hybrid equivalent circuit using an effective capacitance $C_T = C_\pi + [g_m R_C + 1] C_\mu$ at high frequencies.

- (d) Derive expressions for mid-band gain and the lower and upper power half frequencies.
- (e) If the transistor has the following parameters: $C_{\mu} = 27 \text{ pF}$, $\beta_0 = 100$, $r_x = 50 \Omega$ and $f_T = 50 \text{ MHz}$, determine the mid band gain and bandwidth of the amplifier.

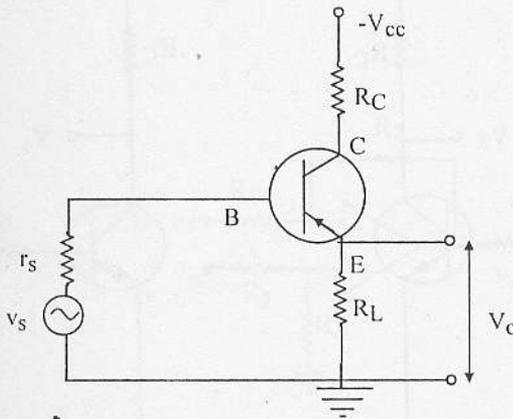
You may find the following information useful.

- $r_{\pi} = \frac{\beta_0}{g_m}$
- $g_m (\text{mS}) = 40 I_C (\text{mA})$
- $C_{\pi} = \frac{\beta_0}{2\pi r_{\pi} f_T} - C_{\mu}$

Here all the symbols have their usual meaning.

2. (a) Explain with the help of a block diagram, the concept of voltage-series feedback.
- (b) Derive expressions for:
- (i) the voltage gain,
 - (ii) the input impedance and
 - (iii) the output impedance
- of a voltage-series feedback amplifier.

(c) The figure shown below is a feedback amplifier.



- (i) Identify the topology.
 - (ii) Draw the basic amplifier circuit without the feedback circuit.
 - (iii) Draw an ac equivalent circuit using the small signal **low frequency hybrid π -model**.
 - (iv) Derive expressions for voltage gain, input impedance and output impedance for the amplifier with feedback.
- (d) Estimate the voltage gain, input impedance and output impedances of the above amplifier, if $r_s = 600 \Omega$, $R_L = 1 \text{ k}\Omega$, $\beta_0 = 100$ and the voltage drop across R_L is 1 V.

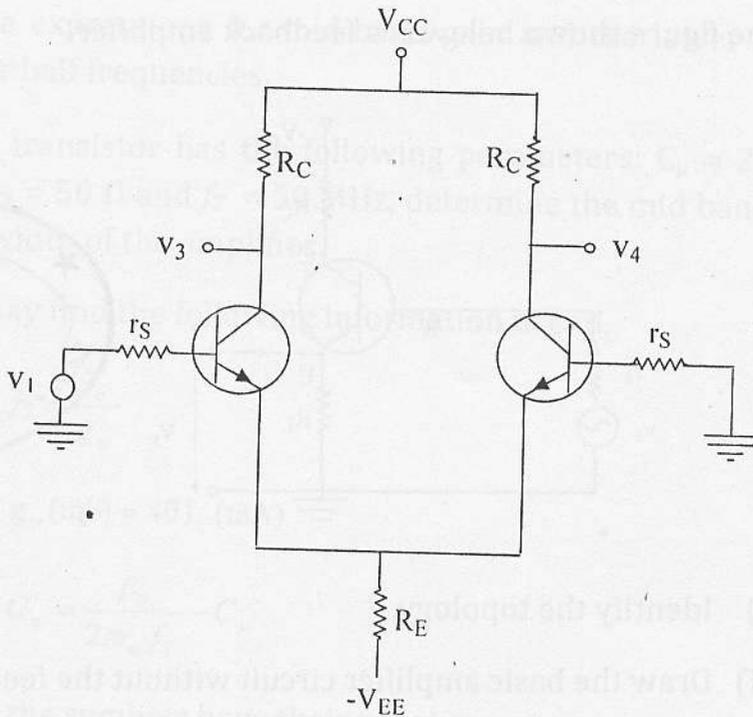
You may find the following information useful.

$$r_{\pi} = \frac{\beta_0}{g_m}$$

$$g_m (\text{mS}) = 40 I_C (\text{mA})$$

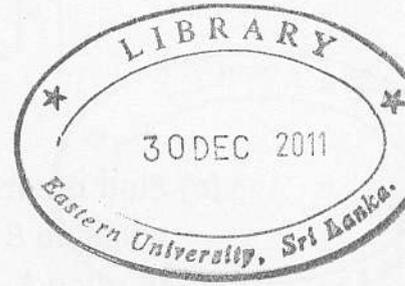
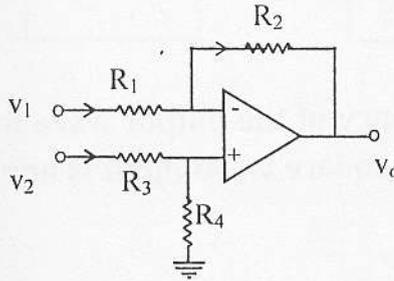
Here all the symbols have their usual meaning.

3. The circuit shown below is a differential amplifier.



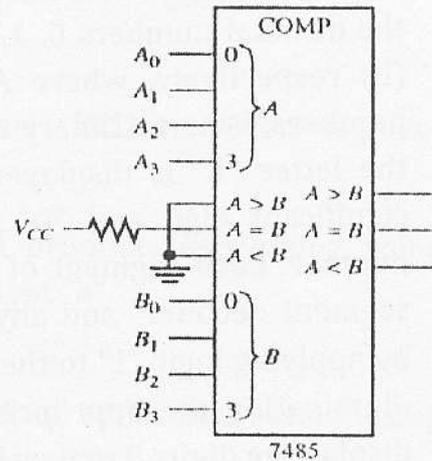
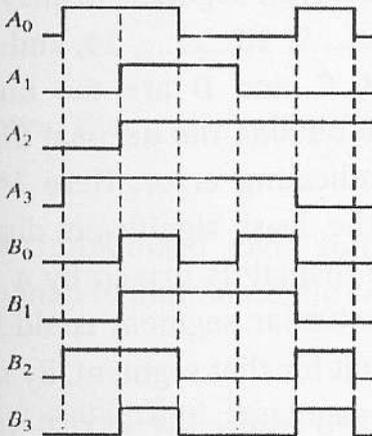
- What do you understand by the term Common-Mode-Rejection-Ratio (CMRR) of a differential amplifier?
- Draw an ac equivalent circuit of the above amplifier using small signal low frequency π -model of the transistor.
- Show that the difference-mode gain is $\frac{-\beta_0 R_C}{2(r_\pi + r_S)}$ when $(\beta_0 + 1)R_E \gg r_\pi + r_S$.
- By recognising the symmetry of the circuit and dividing it into two identical parts, show that the common-mode gain is $\frac{-\beta_0 R_C}{r_\pi + 2(1 + \beta_0)R_E}$.
- Show that the Common-Mode-Rejection-Ratio, $CMRR \approx \frac{-\beta_0 R_E}{(r_\pi + r_S)}$.
- What is the value of R_E , if CMRR of the differential amplifier is 3 dB. You may assume that $\beta_0 = 200$ and $r_S = r_\pi = 1 \text{ k}\Omega$.
- Briefly describe the modification to be made in the circuit to increase the CMRR value.

4. (a) For the following circuit, derive an expression for the output signal in terms of the input signal(s).

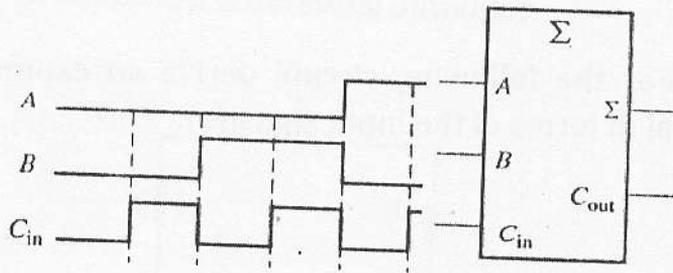


- (b) Hence, design a circuit using operational amplifiers to get voltage source $\sin 3\omega t$, if the voltage sources $\cos^3 \omega t$ and $\sin \omega t$ are available.

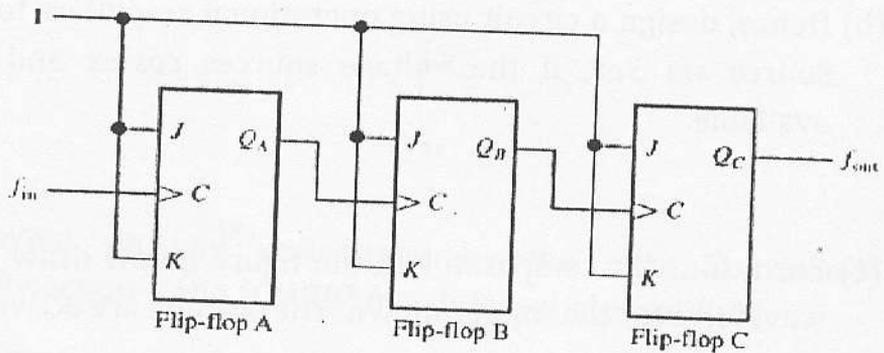
- (c) For a four bit comparator in the figure below draw each output waveform for the inputs shown. The outputs are active-HIGH.



- (d) Draw the output waveform for the inputs of an adder given in the figure below.



(e) Find the frequency of the output wave form for the circuit below when an 8 kHz square wave input is applied to the clock input of flip-flop A.



5. The figure (a) is a layout of a seven segment display for displaying the decimal numbers 0, 1, 2,, 9, 10,....., 14, and 15 as in figure (b) respectively, where A, B, C, and D are the binary inputs of numbers. When a binary code outside the decimal digits is present, the letter "E" is displayed indicating error. Here "A" is the most significant digit and "D" is the least significant digit of a binary number. Each segment of the display is driven by a "BCD to seven segment decoder" and any particular segment could be illuminated by applying logic "1" to the input for that segment. By simultaneously illuminating the appropriate segments, the device can be used to display the digits 0 to 9 or E as shown in the figure (b).

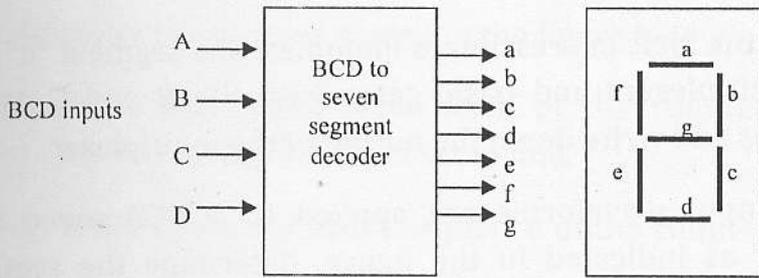


Figure (a)

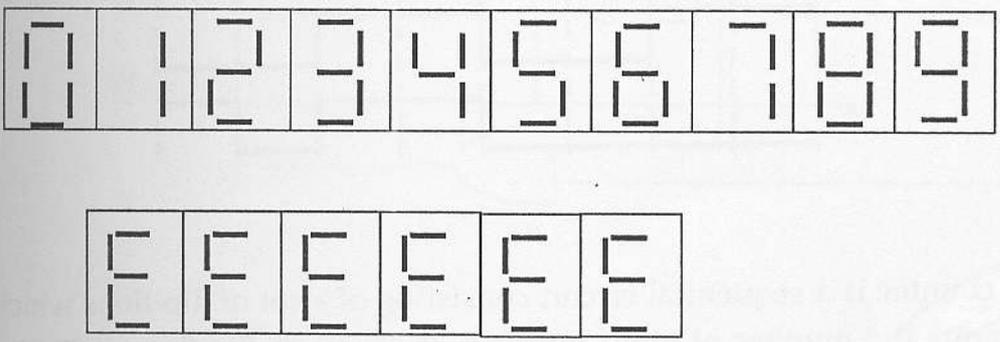
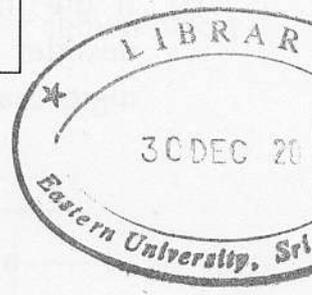
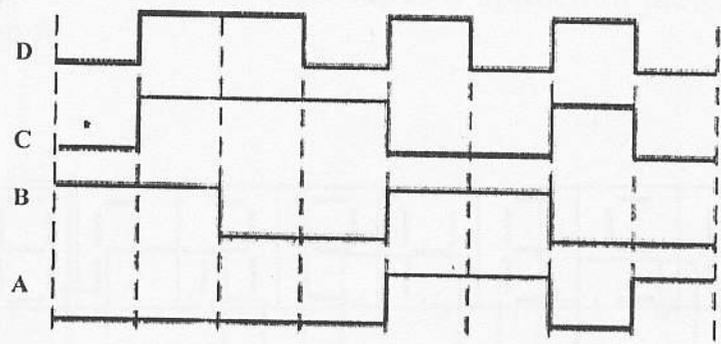


Figure (b)

- (a) Write down the truth table for this "BCD to seven segment decoder".
- (b) Obtain the minimized logic sum of products expression using Karnaugh map to illuminate the segment "e".
- (c) Obtain the minimized logic product of sums expression using Karnaugh map to illuminate the segment "c".
- (d) Realize the logic expression obtained in part (c) using only NAND gates.

- (e) Realize the logic expression to illuminate the segment "d" using 1-of-4 multiplexers and basic gates with the B and D as control variables and write down the output of the multiplexer.
- (f) If the input waveforms are applied to a BCD seven segment decoder as indicated in the figure, determine the sequence of digits that appears on the display.

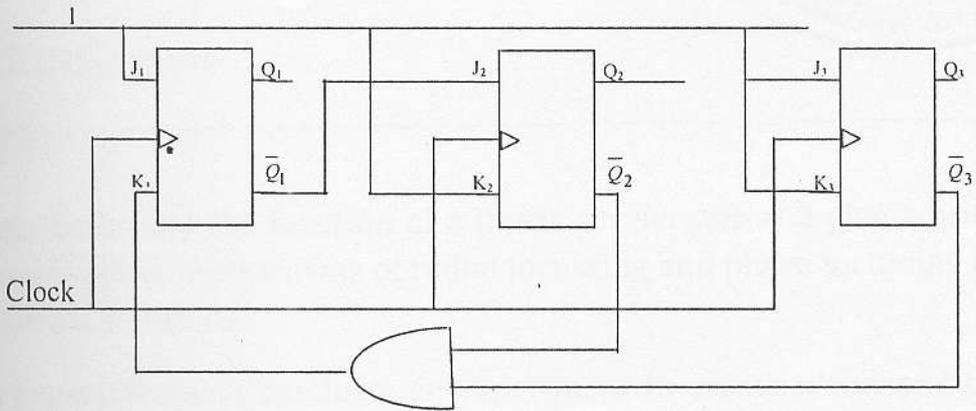


6. A counter is a sequential circuit consisting of a set of flip-flops which counts the number of input pulses it receives. JK flip-flops or T flip-flops are the important building blocks of these counters.
- (a) Write down the truth table for a JK flip-flop.
- (b) Draw a logic diagram for a *decade or mod 10* asynchronous counts counter.
- (c) A binary synchronous counter has the irregular count sequence 1, 0, 3, 4, 5, 6, 1, 0, and uses three falling edge flip-flops.
- (i) Write down the transition table for the three flip-flops.
- (ii) Find a logic expression for the inputs of the above three flip-flops.
- (iii) Draw the logic diagram for the above counter using JK flip-flops with falling edge triggering and digital gates.

(d) Consider the counter shown in the figure below.

(i) Draw the output wave form of the counter. Assume that initially all flip flops are set to one.

(ii) Write down the count sequence of the counter shown below.



You may find the following transition table useful:



| Q_n | Q_{n+1} | J | K |
|-------|-----------|-----|-----|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

X- don't care term