Eastern University, Sri Lanka

Second Examination in Science First Semester – 2000/2001

Computer Organization and Architecture

CS206

Answer all Questions

Time Allowed : Two Hours.

1)

i) A circuit has four inputs A,B,C,D representing the sixteen natural binary integers 0000 (0) to 1111(15). A is the most significant bit and D is least significant bit. The output of the circuit ,F, is true if the input is divisible by multiple of 4,5,6 or 7, with the exception of 15, in which case the output is false. Zero is not divisible by 4,5,6 or 7 .

a) Draw a truth table to represent the algorithm.
b) From the truth table obtain an expression for F and show that

$F=\overline{A}.B+A.\overline{D}$

ii)

a) Describe the construction of a Full Adder.
b) Construct a Parallel Adder Using Full Adders.

2)

i) Describe with the aid of examples, the properties of 2's complement numbers. What is the range of two's complement numbers in n bits and what will happen if we violate this range? Provide examples?

ii) Explain why floating point representation is used in a computer.
A particular computer allocates 16-bits to represent a floating point number, using 6-bit exponent in **excess-32** and 10-bit two's complement **normalized mantissa**.
Explain the meaning of the underlined terms.
Perform the following calculations:

a) 157.3
+ 257.1

b) 157.3
- 142.7

In each case show how the numbers would be stored in the computer.

3) Describe the function of the following registers in a computer:
   i) MAR
   ii) MBR
   iii) PC
   iv) ACC
   v) IR
   vi) Flags

   a) Explain the steps involved in Instruction execution.
   b) Describe, with the aid of a schematic diagram, data flow in interrupt cycle.
   c) Describe the Pipelining technique in the instruction execution of a computer? Illustrate with an Example.

4) What is a Bus in a computer?
   What are the purposes of the following Busses?
   i) Data Bus.
   ii) Address Bus.
   iii) Control Bus.

   a) Describe the sequence of events takes place when memory to processor reading and processor to memory writing.

   b) Illustrate, with the aid of a diagram, the use of a **Cache** memory in alleviating the speed mismatch of memory and processors. Explain the terms **spatial locality** and **temporal locality** of reference of instructions in programs.

   c) Draw a schematic diagram for a DMA transfer from Input to memory and describe the steps involved in the DMA transfer of one word.
   What is cycle stealing?
   Briefly describe the procedure involved in transferring a block of data from a high-speed device such as a disk drive.